SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and hereby claims priority to Japanese Application No. 2006-094576 filed on Mar. 30, 2006 in Japan, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] (1) Field of the Invention

[0003] The present invention relates to a semiconductor device and manufacturing method thereof suitable for use in, for example, a gallium nitride based field effect transistor (GaNFET).

[0004] (2) Description of Related Art

[0005] Recently, development of a GaNFET (gallium nitride field effect transistor) is actively in progress, which makes use of an AlGaN/GaN hetero junction and the electron transit layer of which is GaN (gallium nitride).

[0006] Because of being a material having a wide band gap, a high breakdown electric field strength, and a large saturation electron speed, GaN is highly promising as a material of a high power output device for which a high voltage operation is required.

[0007] At present, for example, for a power device for a mobile phone base station, a high voltage operation of 40 V or higher is required and GaNFET is very promising.

[0008] For such GaNFET as a high power output device, it is necessary to reduce the contact resistivity of source electrode and drain electrode to increase power efficiency.

[0009] Hitherto, a GaNFET has a structure, for example as shown in FIG. **5**, in which a GaN electron transit layer **2** and an $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3** are formed in order on a substrate **1** and a gate electrode **5**, a source electrode **6**, and a drain electrode **7** are provided on the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**. In FIG. **5**, symbol **4** denotes an SiN passivation film.

[0010] Then, as the source electrode **6** and the drain electrode **7** (that is, an ohmic electrode) provided on the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**, a Ti/Al electrode or a Ti/Al/Ni/Au electrode is mainly used.

[0011] As a result of the prior art search, published Japanese translation of PCT International Publication for Patent Application, No. 2005-509274 has been obtained.

[0012] By the way, as described above, in a GaNFET that uses the Ti/Al electrode or the Ti/Al/Ni/Au electrode as an ohmic electrode, the work function of Ti is 4.3 eV, therefore, there is a problem that a Schottky barrier is formed in between with an n-type III-V group nitride compound semiconductor.

[0013] When the Ti/Al electrode or the Ti/Al/Ni/Au electrode is used, a compound is generated at an interface between Ti and Al at the time of annealing to obtain the ohmic properties, and the melting point of the compound is not so high. Further, at the time of annealing, metal condenses, irregularities are formed, and the electrode surface becomes coarse [refer to FIG. **6**(A) to FIG. **6**(D)]. Furthermore, during operation at high temperatures, the Al atom, which is an electrode constituting element, moves (electromigration). These constitute factors that make the ohmic properties unstable at the time of device process or during operation at high temperatures.

SUMMARY OF THE INVENTION

[0014] The inventors of the present invention have proposed one having a Ta/Al lamination structure as an ohmic electrode (for example, refer to Japanese Patent Application No. 2004-353460).

[0015] Specifically, as shown in FIG. **7**(A) and FIG. **7**(B), we have proposed to configure a GaNFET by forming the GaN electron transit layer **2**, the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**, and an n-type GaN layer **8** in order on an SiC substrate **11**, providing the gate electrode **5** on the n-type GaN layer **8**, and providing the source electrode **6** and the drain electrode **7** having a structure (Ta/Al stacked structure) in which a tantalum (Ta) layer **9** and an aluminum (Al) layer **10** are stacked in order on the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**. In FIG. **7**(A) and FIG. **7**(B), symbol **4** denotes an SiN passivation film.

[0016] Due to this, it has been made possible to suppress the electrode surface from becoming coarse [refer to FIG. **8**(A) and FIG. **8**(B)]. Further, it has been made possible to suppress the movement (electromigration) of the Al atom during operation at high temperatures.

[0017] Thus, by using the Ta/Al stacked structure for the source electrode **6** and the drain electrode **7** as an ohmic electrode, it has been made possible to realize sufficient reliability in a high temperature environment.

[0018] However, aluminum (Al) is exposed on the electrode surface, therefore, there is a possibility that the electrode surface is corroded in a high humidity environment.

[0019] Generally, aluminum (Al) turns into aluminum hydroxide by reacting with water in the atmosphere. Since the aluminum hydroxide has a volume three times that of aluminum (Al), damage may be given to the portion (not shown) that covers the surface of the ohmic electrodes **6** and **7** of the SiN passivation film **4**.

[0020] Aspect of the present invention can provide a semiconductor device and manufacturing method thereof that have been made capable of improving reliability of an ohmic electrode in a high humidity environment while securing sufficient reliability of an ohmic electrode in a high temperature environment.

[0021] In accordance with one aspect of the present invention, a semiconductor device comprises a substrate, an n-type semiconductor layer or an undoped semiconductor layer on the substrate, and an ohmic electrode on the n-type semiconductor layer or the undoped semiconductor layer, wherein the ohmic electrode comprises a tantalum layer formed on the n-type semiconductor layer or the undoped semiconductor layer, an aluminum layer formed on the tantalum layer, and a metal layer formed on the aluminum layer and made of any one material of tantalum, nickel, palladium, and molybdenum.

[0022] In accordance with another aspect of the present invention, a method for manufacturing a semiconductor device comprises the steps of: forming at least an n-type semiconductor layer or an undoped semiconductor layer on a substrate; forming a tantalum layer, an aluminum layer, and a metal layer made of any one material of tantalum, nickel, palladium, and molybdenum in order on the n-type semiconductor layer or the undoped semiconductor layer; and annealing at temperatures lower than 600° C., and thus forming an ohmic electrode.